

CLAIMS

What is claimed is:

1        1. In a computer having a peripheral component interconnect (PCI)  
2 system having a host bridge coupling a plurality of PCI slots of a PCI bus to a  
3 processor, the computer accessing base address registers with firmware, a method  
4 of identifying a failing PCI slot, comprising the steps of:

5              (a) creating a firmware maintained PCI resource allocation map in which  
6 addresses for PCI slots associated with the base address registers and sizes of  
7 address ranges for these addresses are mapped;

8              (b) updating the firmware maintained PCI resource allocation map upon  
9 the occurrence of at least of firmware being called to execute at least one of a hot  
10 plug operation and a PCI configuration space transaction; and

11              (c) upon the host bridge logging an error address due to a failing PCI slot,  
12 identifying the failing PCI slot from the information in the firmware maintained PCI  
13 resource allocation map.

1        2. The method of claim 1 wherein upon the occurrence of a hot plug  
2 operation for a PCI slot, a hot plug flag associated with that PCI slot is set and upon  
3 the host bridge logging an error address, invalidating the firmware maintained PCI  
4 resource allocation map entries associated with each PCI slot having its hot plug flag  
5 set.

1           3. The method of claim 2 and further including upon the occurrence of  
2 firmware being called to execute a PCI configuration space transaction, invalidating  
3 the firmware maintained PCI resource allocation map entries associated with each  
4 PCI slot having its associated hot plug flag set and clearing those hot plug flags.

1           4. The method of claim 1 wherein the step of identifying the failing PCI  
2 slot from the information in the firmware maintained PCI resource allocation map  
3 includes identifying the failing PCI slot from an address associated with a base  
4 address register when the logged error address falls within a known address size  
5 range for the address associated that base address register.

1           5. The method of claim 4 wherein the step of identifying the failing PCI  
2 slot further includes identifying the failing PCI slot as unknown when the logged error  
3 address falls after a known address size range of an address associated with that  
4 base address register preceding the logged error address.

1           6. The method of claim 4 wherein the step of identifying the failing PCI  
2 slot further includes identifying the failing PCI slot from the address associated with  
3 that base address register preceding the logged error address when the logged error  
4 address where the address the size range for that preceding BAR is unknown.

1           7. The method of claim 6 wherein the step of identifying the failing PCI  
2 slot further includes identifying the failing PCI slot from the address associated with  
3 that base address register preceding the logged error address when the address the  
4 size for the address associated with that preceding BAR is unknown.

1           8. The method of claim 7 wherein upon the occurrence of a hot plug  
2 operation for a PCI slot, a hot plug flag associated with that PCI slot is set and upon  
3 the host bridge logging an error address, invalidating the firmware maintained PCI  
4 resource allocation map entries associated with each PCI slot having its hot plug flag  
5 set and clearing those hot plug flags.

1           9. The method of claim 8 and further including upon the occurrence of  
2 firmware being called to execute a PCI configuration space transaction, invalidating  
3 the firmware maintained PCI resource allocation map entries associated with each  
4 PCI slot having its associated hot plug flag set and clearing those hot plug flags.

1           10. In a computer having a peripheral component interconnect (PCI)  
2 system having a host bridge coupling a plurality of PCI slots of a PCI bus to a  
3 processor, the computer accessing base address registers with firmware, a method  
4 of identifying a failing PCI slot, comprising the steps of:  
5           (a) creating a firmware maintained PCI resource allocation map in which  
6 addresses for PCI slots associated with the base address registers and sizes of  
7 address ranges for these addresses are mapped;  
8           (b) upon the occurrence of a hot plug operation for a PCI slot, setting a hot  
9 plug flag associated with that PCI slot;  
10          (c) upon the occurrence of at least one of the firmware being called to  
11 execute a PCI configuration space transaction and the host bridge logging an error  
12 address, invalidating the firmware maintained PCI resource allocation map entries  
13 for each PCI slot having its hot flag set; and  
14          (d) upon the host bridge logging an error address due to a failing PCI slot,  
15 identifying the failing PCI slot from an address associated with a base address  
16 register when the logged error address falls within a known address size range for  
17 the address associated that base address register and identifying the failing PCI slot  
18 as unknown when the logged error address falls after a known address size range of  
19 an address associated with that base address register preceding the logged error  
20 address.

1        11. The method of claim 10 wherein the step of identifying the failing PCI  
2 slot further includes identifying the failing PCI slot from the address associated with  
3 that base address register preceding the logged error address when the address the  
4 size range for the address associated with that preceding BAR is unknown.

1        12. In a computer having a peripheral component interconnect (PCI)  
2 system having a PCI to PCI bridge coupling a plurality of PCI slots of a PCI bus to a  
3 processor, the computer accessing base address registers with firmware, a method  
4 of identifying a failing PCI slot below the PCI to PCI bridge, comprising the steps of:  
5            (a) creating a firmware maintained PCI resource allocation map in which  
6 addresses for PCI slots associated with the base address registers and sizes of  
7 address ranges for these addresses are mapped;  
8            (b) upon the occurrence of a hot plug operation for a PCI slot, setting a hot  
9 plug flag associated with that PCI slot;  
10           (c) upon the occurrence of at least one of the firmware being called to  
11 execute a PCI configuration space transaction and the PCI to PCI bridge logging an  
12 error address, invalidating the firmware maintained PCI resource allocation map  
13 entries for each PCI slot having its hot flag set; and  
14           (d) upon the PCI to PCI bridge logging an error address due to a failing  
15 PCI slot, identifying the failing PCI slot from an address associated with a base  
16 address register when the logged error address falls within a known address size  
17 range for the address associated that base address register and identifying the  
18 failing PCI slot as unknown when the logged error address falls after a known  
19 address size range of an address associated with that base address register  
20 preceding the logged error address.

1           13. The method of claim 12 wherein the step of identifying the failing PCI  
2 slot further includes identifying the failing PCI slot from the address associated with  
3 that base address register preceding the logged error address when the address the  
4 size range for the address associated with that preceding BAR is unknown.

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